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Effect of Thermal Oxide Film on Scalable Fabrication of Silicon Nanowire Arrays Using Metal Assisted Chemical Etching

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Effect of Thermal Oxide Film on Scalable Fabrication of Silicon Nanowire Arrays Using Metal Assisted Chemical Etching

by

Mariana Castaneda

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Dedication

Para Ricardo, Guadalupe, Marcela, y Marisol – sin su apoyo, ánimo, y sabiduría sin fin, no estaría donde estoy. Gracias por enseñarme a expandir mis alas y volar.
¡Los amo, y ya puedo pasar por mi diploma!

Para mi abuelo Ezequiel – por enseñarme que la humildad y bondad hacia otros es lo que nos hace humanos, y qué hay todo un mundo que ver, una vida que vivir, y una lección que aprender sin importar la edad.

To my love and best friend Michael – thank you for being home away from home and the best part of my day.
I love you like no other.

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Abstract

Effect of Thermal Oxide Film on Scalable Fabrication of Silicon Nanowire Arrays Using Metal Assisted Chemical Etching

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Over the last several decades, the demand for real-time data processing and storage has exponentially increased and pushed the semiconductor field to its fabrication limits. Traditional methods of semiconductor nanomanufacturing, like lithography and reactive ion etching (RIE), suffer from feature resolution and etch taper limits for devices comprising sub-10 nm nanofabrication nodes. Methods like the ones mentioned above are both expensive and difficult to manufacture to keep up with continued scaling requirements of semiconductor fabrication.

This thesis presents a fabrication method and metrology characterization of silicon nanowire arrays using a Metal Assisted Chemical Etching (MACE) approach. MACE is a simple, low-cost fabrication technique that allows for high aspect ratio silicon nanostructures to be successfully fabricated without sacrificing geometry fidelity, making it a promising etching method for large-scale semiconductor manufacturing.

In this research, small-scale MACE was demonstrated on silicon coupons with an initial process window of 0 nm – 100 nm oxide thickness. Then, a down-selected process

window of 10 nm – 50 nm oxide thickness was successfully reproduced on a full-wafer scale (100 mm diameter silicon wafers) at different etchant solution concentrations. The oxide layer serves as a sacrificial layer between the silicon and resist to allow a consistent etching starting point, thus improving the etch depth uniformity and aspect ratios of silicon nanowires. The silicon nanowires were characterized using local scanning electron microscopy (SEM) images by mapping the areas of the wafer as North, South, East, and West to measure critical dimensions such as height and diameter, as well as to observe phenomena such as nanowire collapse.

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Chapter 1: Introduction

1.1 MOTIVATION

High performance computing and high-density memory have revolutionized all aspects of computing and consumer electronics. Scientific breakthroughs and discoveries in memory and storage have yielded one innovative technology after another, improving the quality of life across the world. As technologies and applications like artificial intelligence (AI), virtual reality (VR), augmented/mixed reality (AR/MR), healthcare, energy efficiency, the Internet of Things (IoT), automation and production, and three-dimensional (3D) imaging evolve, the amount of data that is collected grows exponentially as does the need to store and process the data in real-time.

In recent years, though, continued progress based on Moore's Law has slowed down due to the limitations of two-dimensional (2D) scaling of transistors and the need for ultra-high aspect ratio nanostructures. In the semiconductor industry, two-dimensional or planar fabrication of dynamic random-access memory (DRAM) capacitors has reached its limit of scaled-down features because industry-standard plasma etching and material deposition have an etch taper which cannot scale beyond a certain point. Therefore, nanofabrication has shifted into a three-dimensional or vertical approach by etching a deep trench or hole in the silicon where capacitor material is deposited. This approach increases the capacitance of the cell while shrinking the area that one DRAM cell occupies. The ability to control the geometry of these ultra-high aspect ratio nanostructures reliably and repeatedly over large areas is imperative for applications like the ones mentioned above.

While a 3D roadmap for semiconductor memory, including 3D Flash and deep trench DRAM capacitors, has had early success, it is limited by extremely small feature sizes and etch processes needed for high-aspect ratio structures.

Multiple top-down and bottom-up methods to fabricate silicon nanostructures are now in use, such as plasma etching, reactive ion etching (RIE), vapor-liquid-solid (VLS) growth, and metal assisted chemical etching (MACE). Of those methods, MACE has shown increasing promise as an etching method due to its cost-efficiency, simplicity, and its ability to both etch without a taper effect and efficiently control numerous parameters like cross-sectional geometry, feature diameter, and other critical dimensions (CDs) in silicon nanostructures which are critical for the successful fabrication of memory chips and electronics manufacturing.

1.2 Research Objectives

The work presented here demonstrates deep silicon nanoscale etching using Au as the metal catalyst for metal assisted chemical etching (MACE) in conjunction with a class of ultraviolet (UV) imprint lithography to create high aspect ratio structures. The focus of this research is to utilize varying oxide thicknesses reliably over large areas to create a reliable metal break and etch nanopillars with MACE, while using scanning electron microscopy (SEM) to evaluate the fidelity of nanoscale geometry and critical dimensions, uniform etch depth, and nanopillar aspect ratios. This etching method, compared to traditional and industry-standard etching methods, offers a promising approach to introduce MACE to large-scale applications in the semiconductor industry.

1.3 Outline of Thesis

The chapters are organized as follows: Chapter 2 reviews the literature on state of the art on semiconductor manufacturing, lithography methods, top-down and bottom-up fabrication methods, and limitations of the current process technologies. Chapter 3 explains the MACE process development, experimental details and procedure for sample preparation, varying oxide thicknesses, and full-wafer scale fabrication of silicon nanowire arrays, measurement of silicon nanowire arrays and metrology approach, results, and discussion of results. Finally, Chapter 4 will discuss the conclusions of this work, including future work and capacitor manufacturing.

1.4 Nomenclature

AI – Artificial Intelligence

VR – Virtual Reality

AR – Augmented Reality

MR – Mixed Reality

IoT – Internet of Things

3D – Three-dimensional

2D – Two-dimensional

DRAM – Dynamic Random-Access Memory

RIE – Reactive Ion Etching

VLS – Vapor-Liquid-Solid

MACE – Metal Assisted Chemical Etching

CDs – Critical Dimensions

UV – Ultraviolet

Si – Silicon

SiNW – Silicon Nanowire(s)

J-FIL – Jet-Flash Imprint Lithography

AR – Aspect Ratio

RLT – Residual Layer Thickness

SEM – Scanning Electron Microscopy

HF – Hydrofluoric Acid

H_2O_2 – Hydrogen Peroxide

DI-H_2O – Deionized water

Au – Gold

Ti – Titanium

Chapter 2: Literature Review on State of the Art in Semiconductor Manufacturing

2.1 Introduction and Background of Fabrication Methods

Silicon (Si) continues to be an important material in the semiconductor industry, as it has been the basis for most electronics today. The main reasons for the use of silicon are that silicon devices exhibit better electrical and mechanical properties at room temperature, high-quality silicon dioxide can be grown thermally and patterned [1] to act as an insulator in the device chip, and device-grade silicon is cheaper than other semiconductor materials like gallium arsenide and gallium nitride.

Since the rise of nanotechnology, there has been a continuous effort in the development of fabrication methods to create functional devices at the nanoscale with minimum dimensions of ≤100 nanometers [2,3]. The ability to reliably fabricate silicon nanostructures is imperative for applications like capacitors [4], lithium-ion batteries [5], nanowire-based solar cells [6], memory devices [7], FinFET transistors [8], silicon nanowire-based drug nanocarriers for cancer therapy [9], and other novel applications, as shown in Figure 2.1.

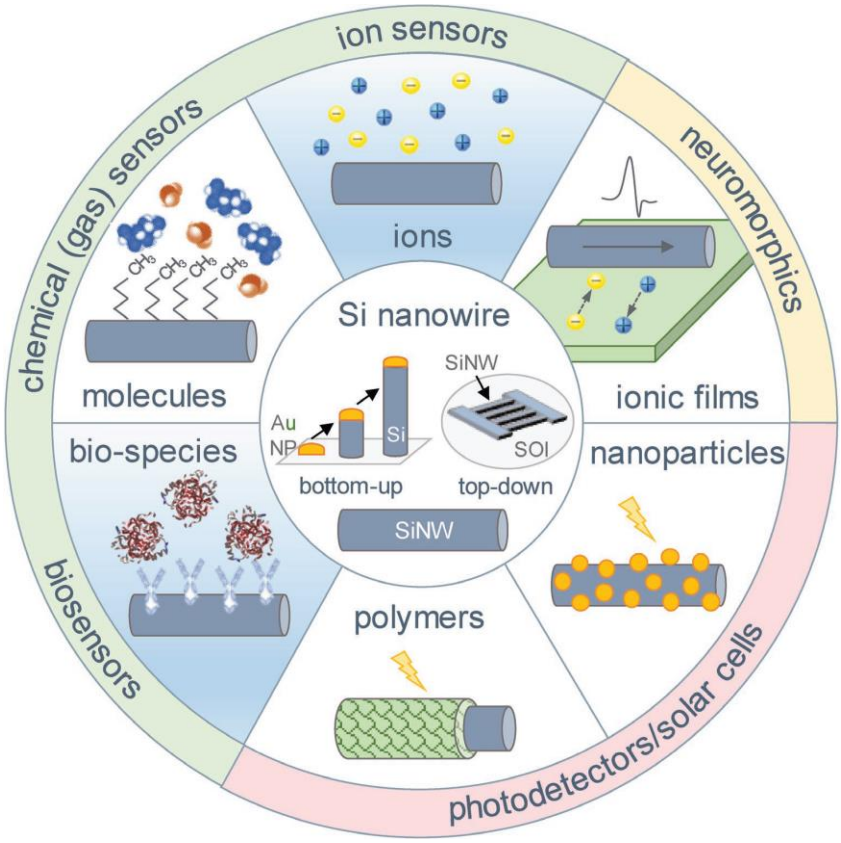


Figure 2.1: From inner to outer layer – silicon nanowire (SiNW) fabrication methods, functional materials on SiNWs, most common SiNW applications [10]

To address the need for silicon nanostructure fabrication, researchers in academia and industry have investigated a variety of fabrication methods over the past few decades. In top-down fabrication, structures are carved from bulk material until a desired shape or structure is achieved. This fabrication method, however, can lead to excessive amounts of material waste and it is usually a more expensive fabrication method. Silicon nanostructures can be fabricated using top-down methods such as patterning coupled with an etch step, plasma etching, reactive ion etching (RIE), and metal assisted chemical

etching (MACE). In the case of top-down fabrication, lithography plays an important and central role to the fabrication of nanostructures. Lithography is the process of transferring patterns of geometric shapes in a mask to a layer of resist that covers the substrate, usually a silicon wafer. On the other hand, bottom-up fabrication creates these shapes/structures by building them up from atomic- and molecular-scale components which can be extremely time consuming [11]. Silicon nanostructures can also be fabricated with bottom-up fabrication methods like chemical vapor deposition (CVD) and Vapor-Liquid-Solid (VLS) growth. Lithography, top-down, and bottom-up fabrication methods are discussed in the following sections to provide an analysis of the current state of the art in nanofabrication within each fabrication method.

2.2 LITHOGRAPHY

Semiconductor lithography is the central step in modern integrated circuit (IC) fabrication because it defines the critical dimension (CD), gate length, of the device. Although lithography is a critical step in IC fabrication, it is both a complex and expensive process to implement. The constant demand to fabricate smaller devices requires lithographic processes to continuously improve a series of parameters: resolution, exposure field, placement accuracy, throughput, defect density, and product yield [12]. Both the throughput and defect density parameters are proportional to the manufacturing cost for finished ICs and yield loss.

2.2.1 Photolithography

Photolithography is a process that allows for the transferring of patterns that define the various areas of integrated circuits like contact windows and implantation regions. In a typical photolithography process, a thin film is deposited on the wafer surface. Then, the thin film is coated with a light-sensitive photoresist. A mask is used to shine UV light through it to project the circuit patterns, and both expose and pattern the resist simultaneously. The resist is then developed and is followed by a selective etching step which leaves the desired pattern of the film on the surface of the wafer.

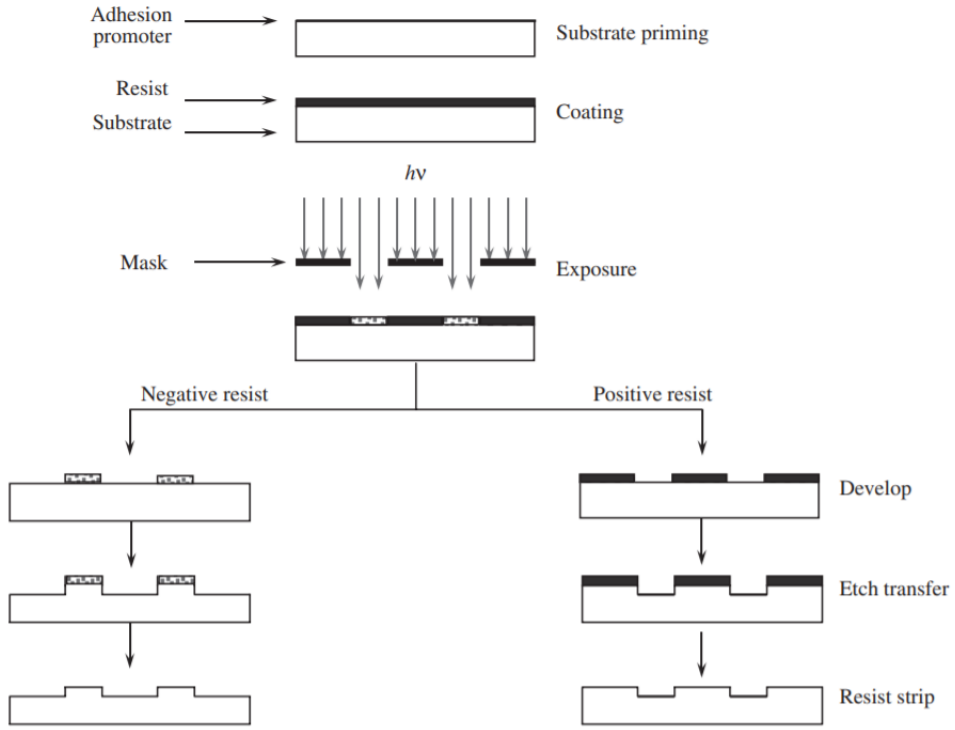


Figure 2.2: Photolithography process showing the use of negative and positive resist [13]

Photolithography is widely used due to its high throughput and good micron-level resolution. But due to deep sub-micron or nanometer IC process requirements, photolithography has faced significant challenges in current process technologies such as

mask alignment concerns due to 3D stacked layers [14] and is tasked to provide better resolution, increase depth of focus (DOF), increase mask manufacturing complexity and reduce the high cost of masks.

2.2.2 Nanoimprint Lithography

Although photolithography has been an established patterning process for many decades, the demand for smaller device features has given significant importance to imprint lithography due to its ability to pattern material over large areas at the nanoscale. To fabricate nanoscale features, there are certain nanoscale manufacturing requirements that must be met: (1) long-range order in nanostructures, (2) patterning structures with varying pattern densities, (3) fabricate multilayered structures with nanoscale overlay, (4) low defect density, and (5) high-throughput over large areas [15]. Early studies have shown sub-10-nm replication resolution [16] and smooth, vertical sidewalls which shows promising nanoscale replication and patterning ability.

Current nanoimprint lithography (NIL) processes are high-resolution and high-throughput processes that can use either a derivation of ultraviolet nanoimprint (UV-NIL) or thermal nanoimprint. Jet and Flash Imprint Lithography (J-FIL) is a type of UV-NIL that uses a transparent template which aids in pattern overlay, is performed at room temperature and low pressures which minimizes distortion and resolution errors, and has shown resolutions to be better than 10 nm [17].

In a typical J-FIL process, ink jets dispense imprint resist onto the substrate. Then, the patterned template or “mask” is lowered onto the substrate with imprint resist which

fills the pattern. The imprint resist is then exposed to and cross-linked with UV light. Finally, the template is separated from the substrate, revealing the desired patterned resist as shown in Figure 2.3. This nanoscale resolution in conjunction with its ability for high throughput makes J-FIL an ideal candidate for the patterning of high aspect ratio silicon structures.

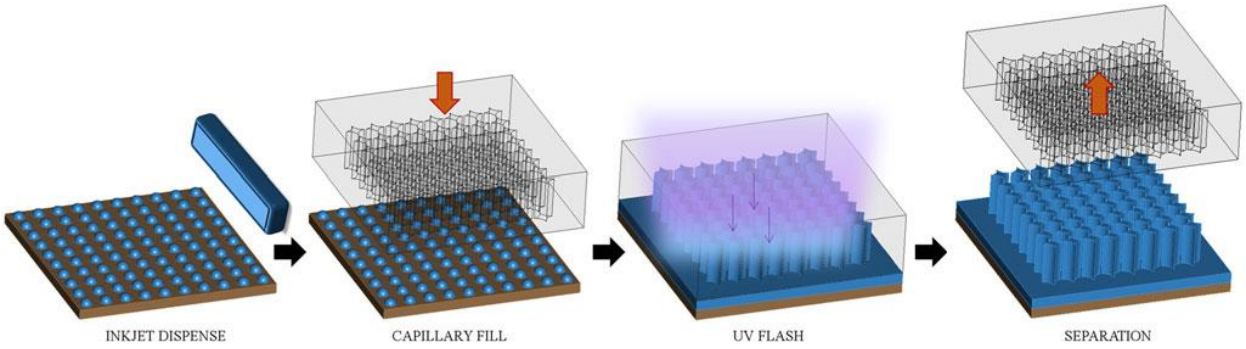


Figure 2.3: Jet-Flash Imprint Lithography process [4]

2.3 Top-Down Fabrication Methods

Immediately following the patterning step, an etching process is used to reliably transfer the pattern created on the resist onto the underlying substrate; for this study, the underlying substrate is silicon. There are two kinds of etching processes: (1) dry etching and (2) wet etching. Dry etching involves the use of etchant gases or plasma to remove exposed substrate material with chemical reactions and accelerated ion bombardment. In contrast, wet etching involves immersing the patterned resist substrate in an etchant solution where exposed substrate material is removed by a chemical reaction. One of the main characteristics that makes dry etching an attractive etching system is that it can define small feature size of <100 nm [18]. However, certain dry etching methods have significant disadvantages at sub-50 nm geometries, including when deep etching is required. MACE

has shown capability in fabricating devices with sub-10 nm feature sizes [4], has lower etchant material costs, simpler equipment requirements, higher etching rates, has higher anisotropy than dry etching, and higher material selectivity [19]. It does have some important limitations, including that it has only been broadly used to etch single crystal silicon. This thesis focuses on a scalable etch process for single crystal silicon at sub-100 nm geometries.

2.3.1 Plasma Etching

Plasma etching was first introduced into the semiconductor industry in the 1970s to achieve selectivity in integrated circuit manufacturing that were difficult to obtain otherwise with wet etching. Plasma etching played a key role in enabling the complex circuit patterns printed by photolithography on polymers to be transferred onto silicon, dielectrics, and other metals that integrated circuits are composed of [20]. This method is used to fabricate anisotropic high aspect ratio nanostructures, but plasma etching fabrication suffers from key challenges like feature sidewall etch taper, Aspect Ratio Dependent Etching (ARDE), and plasma induced sidewall damage.

In a typical plasma etching process, the patterned substrate is placed within a low-pressure vacuum chamber where an etching gas is introduced. Then, radio frequency (RF) energy from an RF power supply is supplied to the top electrode in the chamber, usually operating at 13.56 MHz. The applied RF causes gas molecules to vibrate at high frequencies that result in an ionized gas species that creates the plasma that is used to etch the substrate.

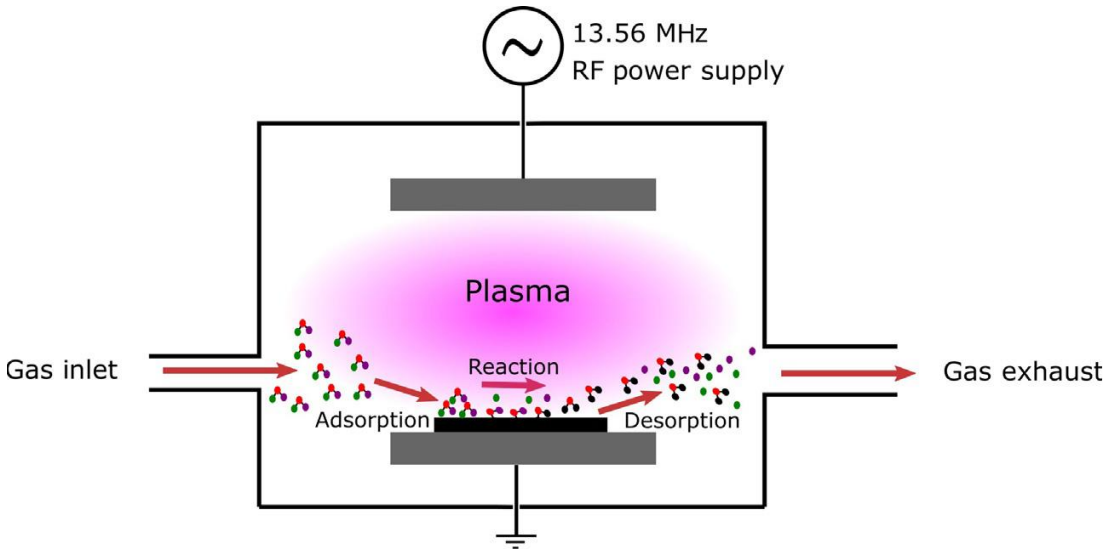


Figure 2.4: Schematic diagram of RF-plasma etch system [21]

2.3.2 Metal Assisted Chemical Etching

This silicon nanowire fabrication study will focus on the nanoimprint lithography method Jet-Flash Imprint Lithography or J-FIL, in conjunction with a wet etching technique called metal assisted chemical etching or MACE. MACE is an electroless wet etching process where silicon is preferentially etched at the interface between a patterned noble metal and the silicon surface in a solution of hydrofluoric acid (HF), DI water, and an oxidant (commonly H_2O_2). This results in an anisotropic, directional etch where the geometry of the features is determined by the shape of the patterned noble metal as well as the metal's mechanical stability during the etch. The preferential etch mechanism is as follows: (1) the noble metal catalyzes the reduction of the oxidant creating holes, (2) the holes are injected through the metal into the silicon where it contacts the metal, (3) the silicon oxidizes, (4) the HF dissolves the oxidized silicon, and (5) finally, the soluble

products are removed and the metal moves into the space where the process repeats shown in Figure 2.5 [22].

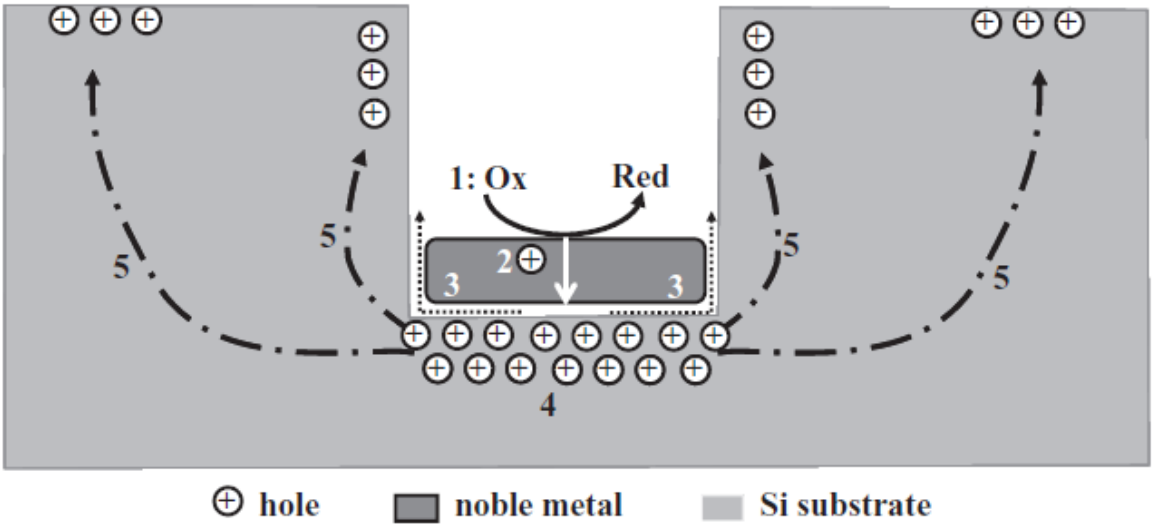


Figure 2.5: Schematic of metal assisted chemical etch mechanism

The characteristics that make MACE an exemplar etching method is that it can sustain critical dimensions for high aspect ratio silicon nanostructures ranging from sub-10 nm to hundreds of microns without sidewall taper effect, and with smooth sidewalls unlike plasma etching. To obtain ideal silicon nanostructures, the uniformity, etch rates, and morphology can be controlled by optimizing a series of parameters that include: the dopant type in the silicon substrate, catalyst material [23], geometry and thickness of the metal catalyst [24], etchant ratios and wettability [25], and temperature [26]. The MACE process development will be explained in further detail in the following chapter.

2.4 Bottom-Up Fabrication Methods

Bottom-up fabrication uses physical and chemical forces at the nanoscale level to assemble individual atoms into larger structures. Unlike top-down fabrication methods

though, bottom-up approaches are used to fabricate periodic structures with circular cross-sections like silicon nanowires and lack long-range order. They cannot be used to fabricate complex structures with varying dimension scales and thus limit the nanostructure designs.

2.4.1 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a process that involves the reaction of volatile precursor gases. The chamber is heated to a reaction temperature that causes the precursor gases to react or break down into the desired coating material and bond to the surface of the substrate. Over time, the coating material builds on the substrate surface and creates a coating throughout the exposed part's surface. CVD processes include Atmospheric Pressure Chemical Vapor Deposition (APCVD) Low-Pressure CVD (LPCVD) with the LPCVD process being the most used method today. CVD processes suffer from major fabrication disadvantages compared to top-down fabrication methods such as specific properties of the precursor gases, high temperature requirement, and coating size limitation due to chamber capacity [27], [28].

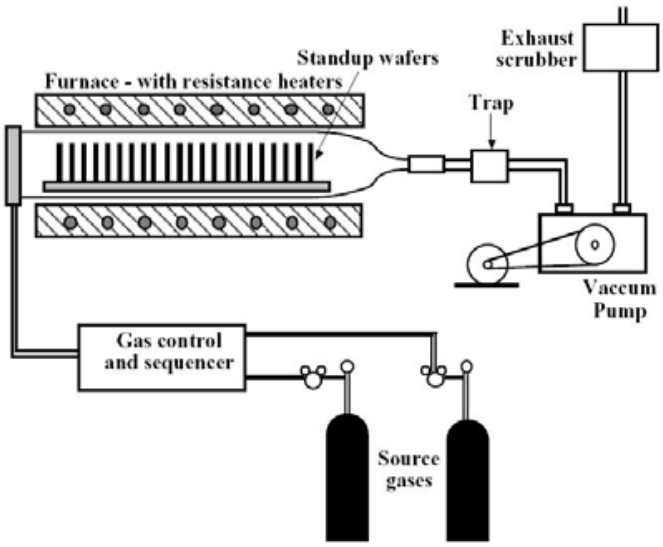


Figure 2.6: Schematic diagram of LPCVD [29]

2.4.2 Vapor-Liquid-Solid Growth

Vapor-Liquid-Solid (VLS) growth is a mechanism that allows the growth of one-dimensional structures, specifically nanowires, from CVD. A typical VLS mechanism is composed of the preparation of a liquid metal-alloy droplet on the substrate surface from where a nanowire will grow, the substance is grown as a vapor which adsorbs onto the liquid surface and then diffuses into the droplet, followed by the supersaturation and nucleation at the liquid/solid interface leading to crystalline nanowire growth [30]. Like CVD, VLS suffers from a major challenge in that nanowire growth is extremely slow. This slow growth affects the ability of high throughput and raises the cost of devices fabricated with VLS.

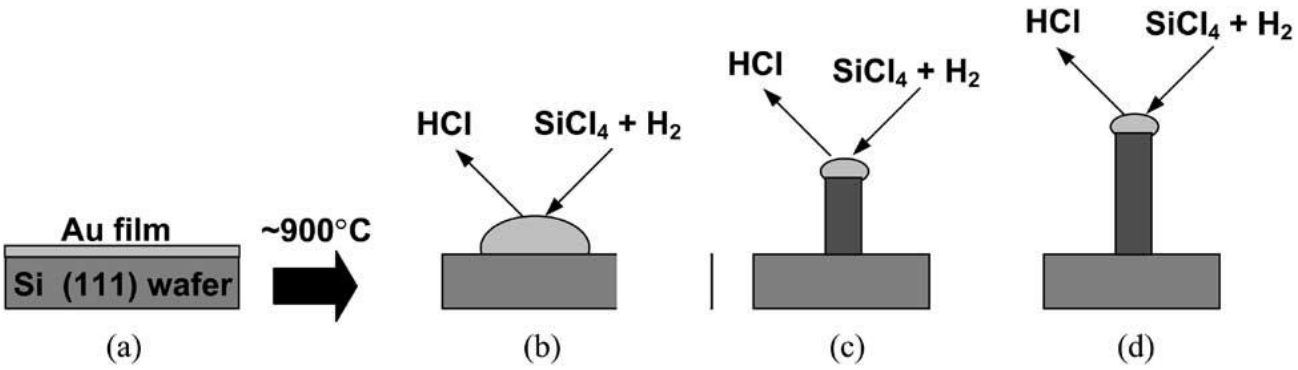


Figure 2.7: Schematic diagram showing Si nanowire growth by VLS [31]

2.5 Summary of Limitations of Current Manufacturing Process Technologies

Although there are multiple top-down and bottom-up silicon nanostructure fabrication techniques, there are several limitations of what is most used today. In particular, industry-standard etching techniques suffer from major challenges like feature sidewall etch taper, Aspect Ratio Dependent Etching (ARDE), plasma induced sidewall damage, as well as limitations in the geometry complexity of silicon nanostructure fabrication at sub-50 nm feature sizes and high-aspect ratio etching. However, MACE has shown promise in the ability to overcome the challenges mentioned above, and provide a simple, cost effective etching method that addresses the need for high aspect ratio nanostructures. MACE has the potential of becoming an industry standard etch technique for deep etching of single crystal silicon.

Chapter 3: Fabrication of Silicon Nanowire Arrays by Metal Assisted Chemical Etching

3.1 Metal Assisted Chemical Etching Process Development

In this study, a method demonstrating the fabrication of silicon nanowire (SiNW) arrays is presented[1]. A Si wafer was patterned with nanoimprint lithography (J-FIL), and the SiNW arrays were etched with a MACE process. This method uses noble metal catalyst patterning to induce local oxidation and reduction reactions for MACE. Both the pattern uniformity and pattern defectivity are characterized by top-down and cross-section scanning electron microscope (SEM) images.

A typical MACE process comprises a metal catalyst patterned on a silicon wafer immersed in a MACE etchant solution. In this study, the MACE etchant solution is composed of HF and H_2O_2 appropriately diluted with DI-H_2O. In the rest of this study, the etchant composition is denoted using molarity which is defined as:

$$Molarity\ (M)\ of\ a\ component = \frac{moles\ of\ solute\ (mol)}{liters\ of\ solution\ (L)} \tag{3.1}$$

The solvent added to achieve desired molarity is DI-H_2O. For example, 12.5 M HF mixed with 1 M H_2O_2 is a common chemistry used in this research. For this study, H_2O_2 was the chosen oxidant and Au was the chosen noble metal catalyst. In the working mechanism of

[1] Individual contributions to this work include thermal oxide growth and ellipsometry to determine oxide thickness, assist in the development of the metal break process for Au patterning, metal catalyst deposition using e-beam evaporation, and small-scale local SEM metrology to characterize nanowire arrays.
[32] A. Mallavarapu, B. Gawlik, M. Grigas, M. Castañeda, O. Abed, M. Watts, S.V. Sreenivasan, "Scalable Fabrication and Metrology of Silicon Nanowire Arrays made by Metal Assisted Chemical Etching," *IEEE Transactions on Nanotechnology*, Submitted July 2020.

a MACE process, the metal catalyst (Au) serves as a cathode to catalyze the reduction of oxidants (H_2O_2) which produces positively charged holes h+. The generated holes diffuse through the Si/metal interface and oxidize the silicon substrate. The excess h+ concentration at the Si interface results in a higher etch rate compared to HF etching on bare Si. HF both dissolves the oxidized Si and diffuses along the sides and through the metal catalyst to etch the oxidized Si. The etched byproducts are soluble and diffuse away. Huang et al. demonstrated a MACE process using Si, HF, and H_2O_2 that can generate hydrogen gas in the redox reaction represented below:

$$Si + \frac{n}{2}H_2O_2 + 6HF \xrightarrow{Catalyst} H_2SiF_6 + nH_2O + \frac{4-n}{2}H_2 \uparrow \qquad (3.2)$$

where n is 2<n<4 and is determined by the ratio of oxidant to HF, which governs the etch domain. Figure 3.1 shows a typical MACE process flow starting with the imprint of nanofeatures, residual layer thickness (RLT) etch (descum), followed by deposition of the metal catalyst, and ending with MACE of silicon nanowire arrays without the removal of Au catalyst and remaining resist caps.

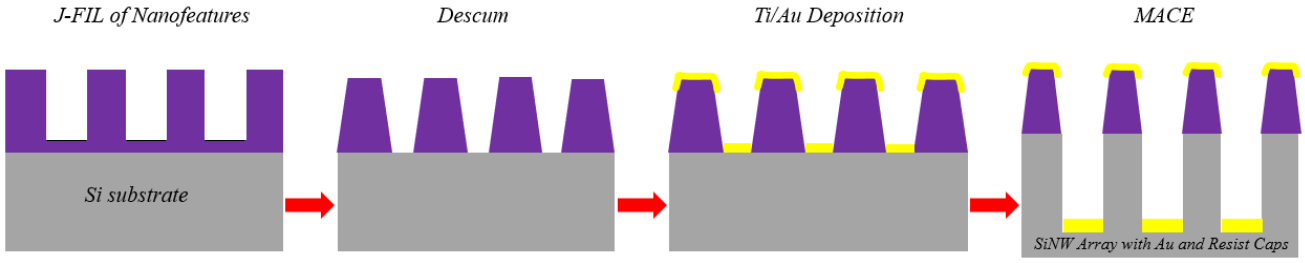


Figure 3.1: MACE process flow for SiNW fabrication with J-FIL and MACE

Gold (Au) was chosen as the noble metal catalyst in this study because this particular metal has to-date demonstrated the best process performance in the sense of

porosity-free, high quality anisotropic etching as compared to other catalysts like platinum (Pt) and palladium (Pd) [33], [34], [35], [36]. Additionally, Au is the most used metal catalyst in current MACE literature [22], [6]. However, there are concerns with using Au as the metal catalyst. The first concern is that Au is not CMOS-application compatible due to the defects in Si that occur because of Au diffusion. Still, this diffusion-induced defect occurs at temperatures of ≥ 200℃ [37]. It is important to emphasize that the MACE process is a room-temperature process, and in this study, the remaining Au on the wafers was fully removed after etching. Therefore, Au diffusion is not a pressing concern in this research. Although Au has: (1) a better process window than other catalysts, (2) high electrical and thermal conductivity, and (3) is resistant to corrosion, it still poses issues with reliable patterning of nanoscale structures. Low volatility of Au during plasma etching can cause certain etch products to redeposit along the sidewalls of nanoscale features which affect the overall geometry and create etch defects [38].

Lift-off is a widely used process for patterning Au in semiconductor fabrication. The lift-off process uses a resist undercut to create a metal break in the deposited Au film. However, removing this sacrificial layer can cause metal catalyst redeposition on nanofeatures during etching which can cause defect and yield problems in manufacturing applications.

Although developing a reliable metal break with J-FIL is challenging, it is highly desirable for manufacturing applications. For the MACE process presented in this study, the lift-off step is eliminated because the metal catalyst (Au) is in direct contact with only the silicon that will be etched. This direct Si/metal catalyst contact along with a metal break

in Au deposition enables manufacturing-friendly MACE. In this research, a silicon dioxide metal-break layer was thermally grown between the resist and the silicon. This oxide layer was explored to allow the etch to begin at the same time across the entire wafer and ensure etch depth uniformity and consistency [32]. The oxide layer between the resist and silicon is hydrophilic and is etched by the HF contained in the MACE solution. Furthermore, a reliable metal break across the wafer appears to be enabled by the oxide layer which not only improves overall etch uniformity significantly and allows for complete metal catalyst removal post-etch, it also ensures the MACE process to not suffer from catalyst redeposition (as is the case in lift-off) during etching which results in yield loss in manufacturing.

3.2 Experimental Details and Procedure

For this study, 100 mm diameter p-type, Boron doped (100) Si wafers with a resistivity of 1-10 Ohm-cm were purchased from UniversityWafer, Inc. A piranha clean was performed on the wafers and was composed of H_2O_2:H_2SO_4 (2:1). The piranha solution was heated for 3 minutes, and the wafers were cleaned for 8 minutes and rinsed with 5 cycles of DI-H_2O, and dried with a dry air supply. Oxide was thermally grown on the wafers with an annealing gate oxide furnace for thicknesses of 10 nm, 20 nm, 30 nm, 50 nm, and 100 nm using a temperature of 950℃ for 10 nm-50 nm oxide thicknesses, and 1100℃ for 100 nm oxide thickness. The growth times were 5 minutes, 20 minutes, 60 minutes, 110 minutes, and 50 minutes, respectively. A J.A. Woolham M-200 DI Ellipsometer was used to confirm the different oxide thicknesses.

After the thermal growth of oxide, each wafer was spin coated at 4000 RPM with an adhesion layer (Transpin®) for 60 seconds and baked at 170℃ for 2 minutes. The wafers were patterned using an IMPRIO 1100 Jet and Flash Imprint Lithography tool. Circular pillars with a diameter of 120 nm and a pitch of 200 nm were imprinted on the wafers. The template consists of 1 mm x 1 mm square dies of nanowire arrays distributed over the 100 mm wafer (see Figure 3.2b below). The residual resist layer of ~10-20 nm was removed or descumed by an oxygen plasma on a Trion RIE etcher for 50 seconds using the following recipe: 15 mT pressure, 65 W power, 70 sccm Ar, and 5 sccm O_2. Metal deposition followed after descum. A 2 nm titanium (Ti) adhesion layer and a 10 nm gold (Au) layer were deposited on the patterned wafers using an electron beam evaporation tool at a pressure of 5.5E-6 torr with deposition rates of 0.2 Å/s and 0.4 Å/s, respectively.

The patterned wafers were then immersed for 30 seconds in a MACE solution composed of 12.5 M HF and 1 M H_2O_2. The etch was subsequently quenched in a bath of H_2O and dried using an air gun with dry air. The Au catalyst was removed using a potassium iodide Au etchant, and the remaining resist was removed using an oxygen plasma. The resulting etched SiNWs are characterized using scanning electron microscopy (SEM) as shown in Figure 3.2 by top-down and cross-section views at the North, South, East, and West locations of the wafers.

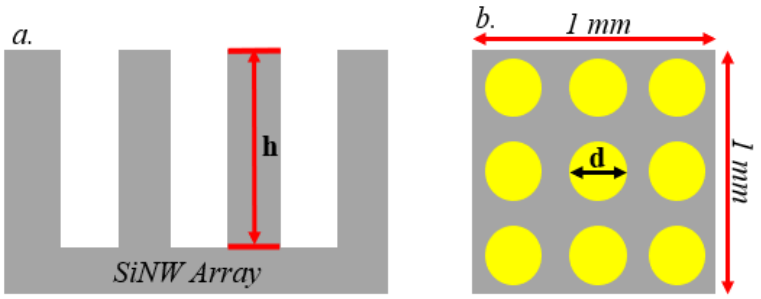


Figure 3.2: a) Cross-section view of SiNW arrays depicting SEM nanowire height measurements and b) Top-down view of 1 mm^2 of SiNW arrays depicting SEM nanowire feature diameter measurements

3.3 RESULTS

3.3.1 Process Window Selection

In the metal break process that was developed for this study, the lift-off step was eliminated. Oxide layers of varying thicknesses were thermally grown to provide a consistent starting point for MACE that ensured etch depth uniformity. A process window of 0 nm – 100 nm oxide thickness were chosen to study for the metal break process on small-area Si coupons. The 0 nm oxide thickness refers to the native oxide that forms on the surface of the Si wafers without additional thermal oxide growth. Additionally, defect modes such as nanofeature collapse are important in order to identify the optimum oxide thickness for this MACE process. Figure 3.3 shows how the Si wafers were cleaved to obtain eight small coupons, and identifies the patterned region of the wafer, as well as defects that occurred during the nanoimprint step. Coupon A6 was used to determine the MACE process window for full-wafer MACE. Table 3.1 shows the results of the process window of 0 nm – 100 nm with local SEM images and SiNW diameter and height measurements.

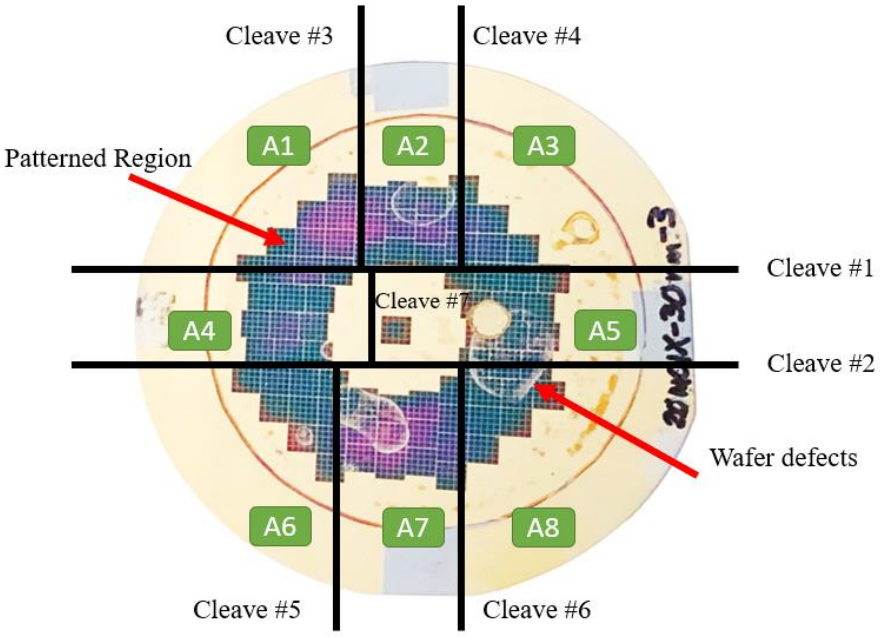


Figure 3.3: 100 nm Si wafer showing the patterned region, wafer defects, and cleave markings to obtain small-area coupons A1-A8

Table 3.1: Initial process window of 0 nm-100 nm oxide thickness

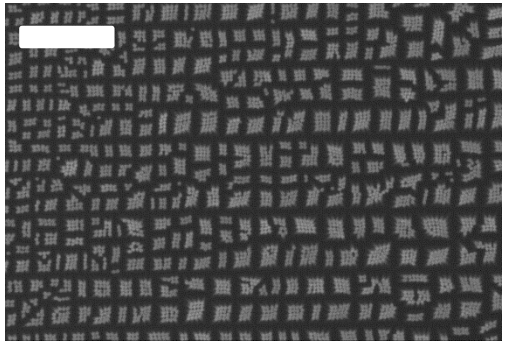
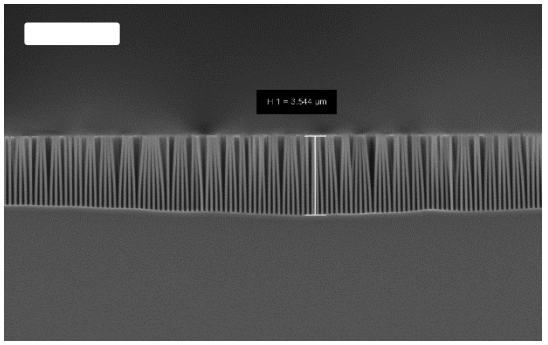
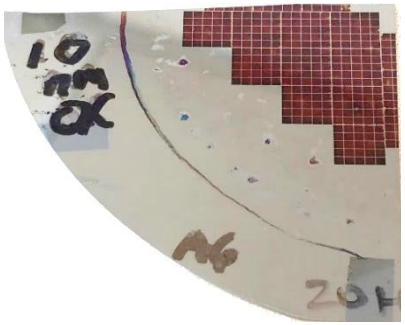
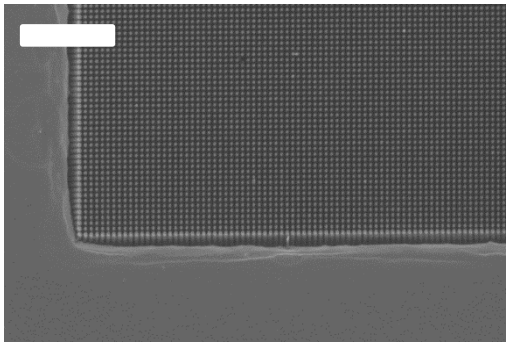
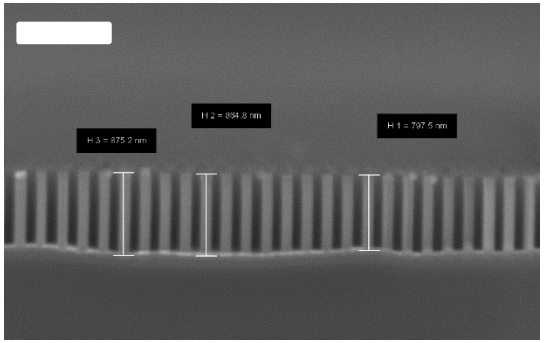
MACE A6 Si-wafer Coupons	Top-Down View Scale bar: 1µm	Cross-Section View Scale bar:1µm	Diameter *d*, Height *h* (nm)
 0 nm			Avg. Diameter = 116.1 nm Avg. Height = 1303.4 nm Collapse = Y
 10 nm			Avg. Diameter = 117.2 nm Avg. Height = 836.82 nm Collapse = N

Table 3.1 (continued)

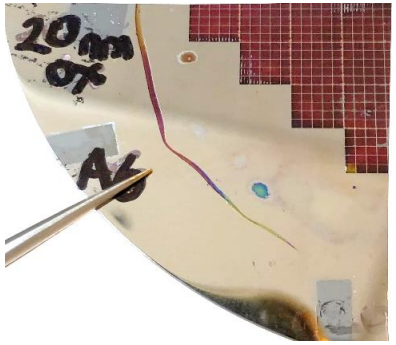
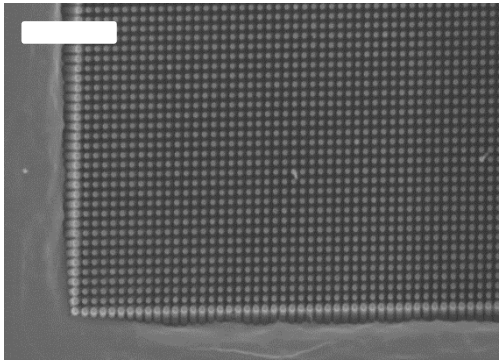
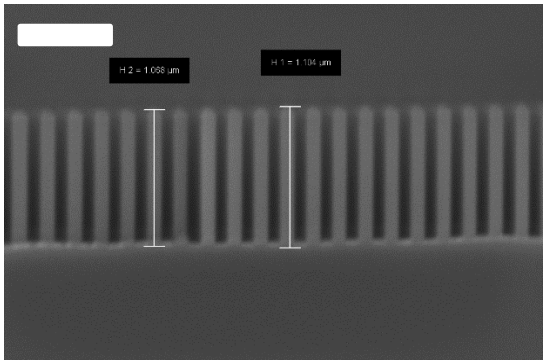
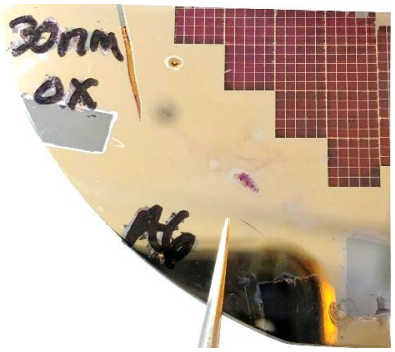
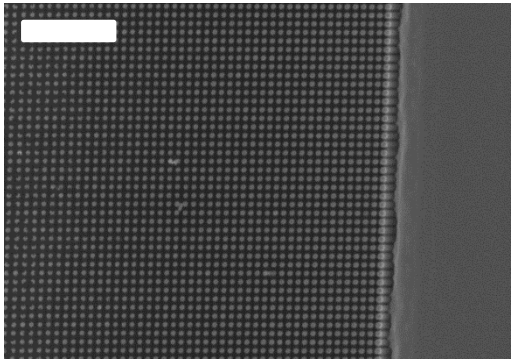
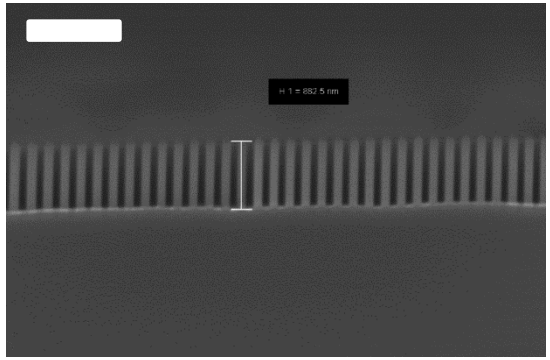
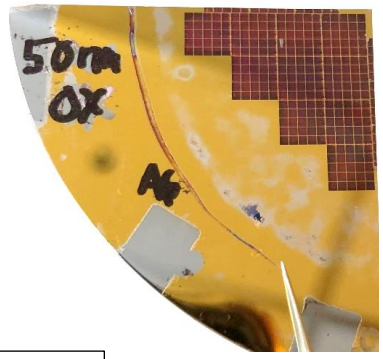
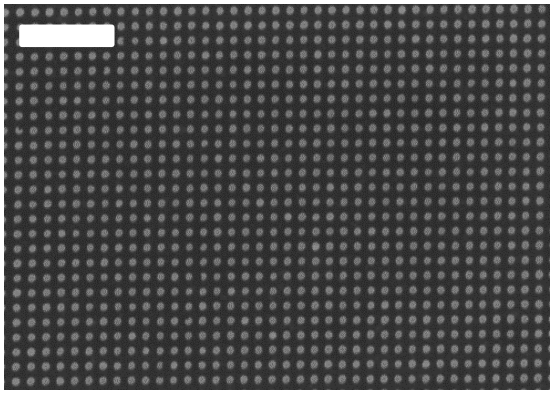
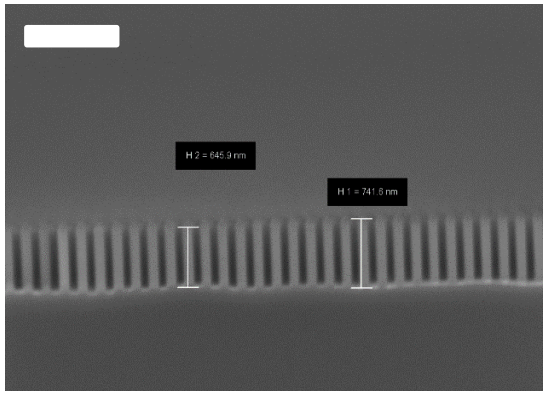
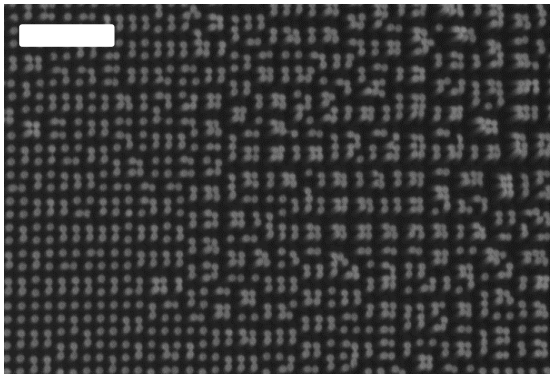
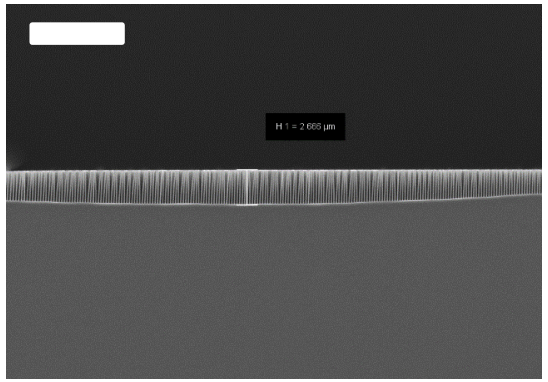
 20 nm			Avg. Diameter = 119.1 nm Avg. Height = 967.20 nm Collapse = N
 30 nm			Avg. Diameter = 118.3 nm Avg. Height = 927.70 nm Collapse = N

Table 3.1 (continued)

 50 nm			Avg. Diameter = 118.8 nm Avg. Height = 707.15 nm Collapse = N
 100 nm			Avg. Diameter = 126.6 nm Avg. Height = 3041.7 nm Collapse = Y

The MACE solution concentrations for this process window were 12.5 M HF and 1 M H_2O_2. Each coupon was dipped into the MACE solution for 30 seconds. The concentration of the MACE solution allowed for a high-speed etch to occur (>0.5 micron per minute), which led to the fabrication of high aspect ratio SiNWs. While the 0 nm (native) oxide and 100 nm oxide thicknesses yielded average SiNW heights of 1303.4 nm and 3041.7 nm, the observed nanowires were collapsed, and etch depth variation was prominent throughout the sample as observed with SEM. On the other hand, the 10 nm – 50 nm oxide layers averaged slightly shorter NWs (707.15 nm – 967.2 nm), but no collapse was observed. Nanowire collapse can occur after MACE when the Si wafer or coupon are removed from the MACE solution and dried. The high aspect ratio of the NWs results in adhesive and capillary forces during the drying process [39]. These adhesive and capillary forces cause the NWs to collapse onto each other because as aspect ratio increases, the mechanical stiffness of SiNWs lowers which creates "bundles" of SiNWs as observed in 0 nm and 100 nm top-down SEM images of Table 3.1.

3.3.2 Full-Wafer Scale MACE

From the process window in the previous section (0 nm – 100 nm), the window that had uniform and no collapsed SiNWs after MACE was from 10 nm – 50 nm (see Table 3.1). Figure 3.4 a) shows the MACE process flow with a layer of oxide between the Si substrate and the resist in thicknesses of 10 nm, 20 nm, 30 nm, and 50 nm, while b) and c) show each MACE process with different HF/H_2O_2 concentrations. The following MACE experiments were conducted on a total of eight 100 mm Si wafers and include (1) one

MACE process of four wafers using the same HF and H_2O_2 ratio and concentration as the Si coupons (12.5M HF and 1M H_2O_2) for a 30 second etch, and (2) one MACE process using four wafers with a diluted HF/H_2O_2 concentration (6.25 M HF and 0.5 M H_2O_2) for a 30 second etch.

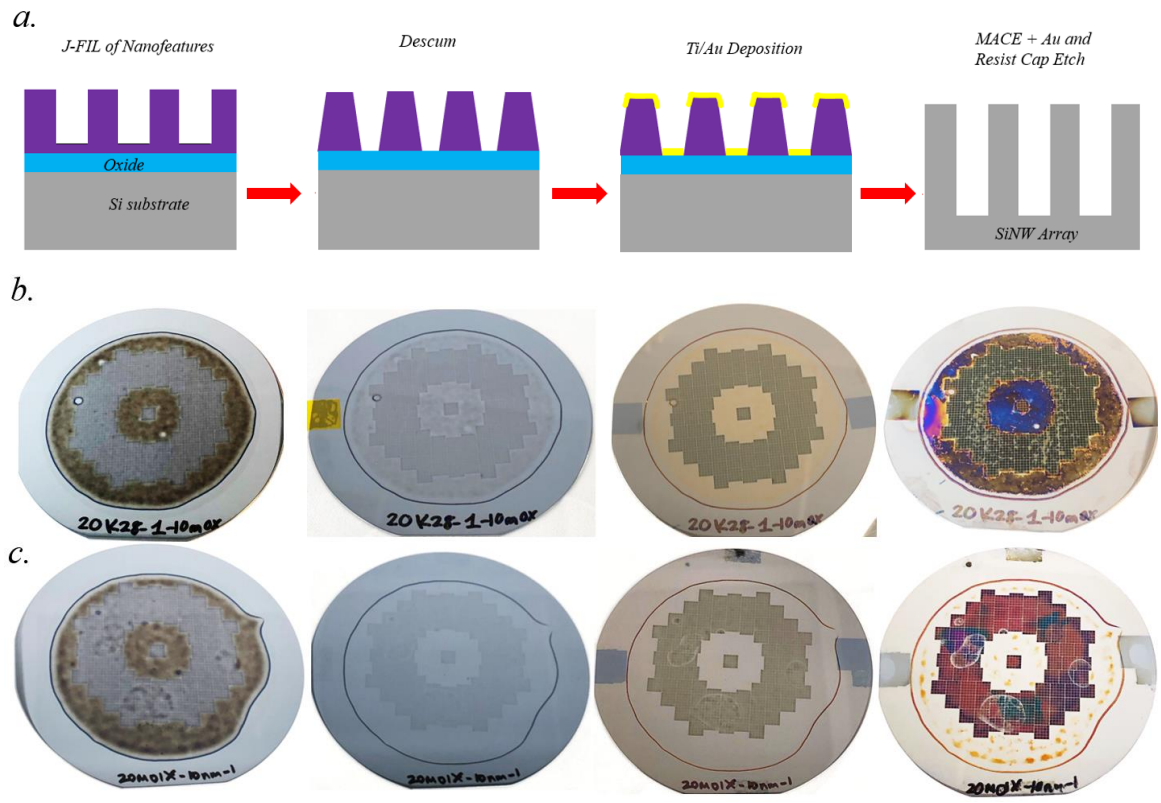


Figure 3.4: a)Full-wafer MACE process flow with layer of oxide varying in thickness from 10 nm, 20 nm, 30 nm, and 50 nm, b) Full-wafer MACE process flow images of 10 nm oxide thickness with etchant composition of 12.5M HF and 1M H_2O_2 after each process step, c) Full-wafer MACE process flow images of 10 nm oxide thickness with etchant composition of 6.25M HF and 0.5M H_2O_2 after each process step

The SiNWs were characterized and measured by mapping the sections of the wafer as North, South, East, West with local SEM images taken in top-down and cross-section views to measure SiNW diameter and height as shown in Figure 3.2. The following figures

(Figures 3.5 – 3.12) show each wafer (10 nm – 50 nm oxide of both MACE solution concentrations) post-MACE with top-down and cross-section views for each cardinal location of the wafer. The scale bar of all SEM images is 1μm.

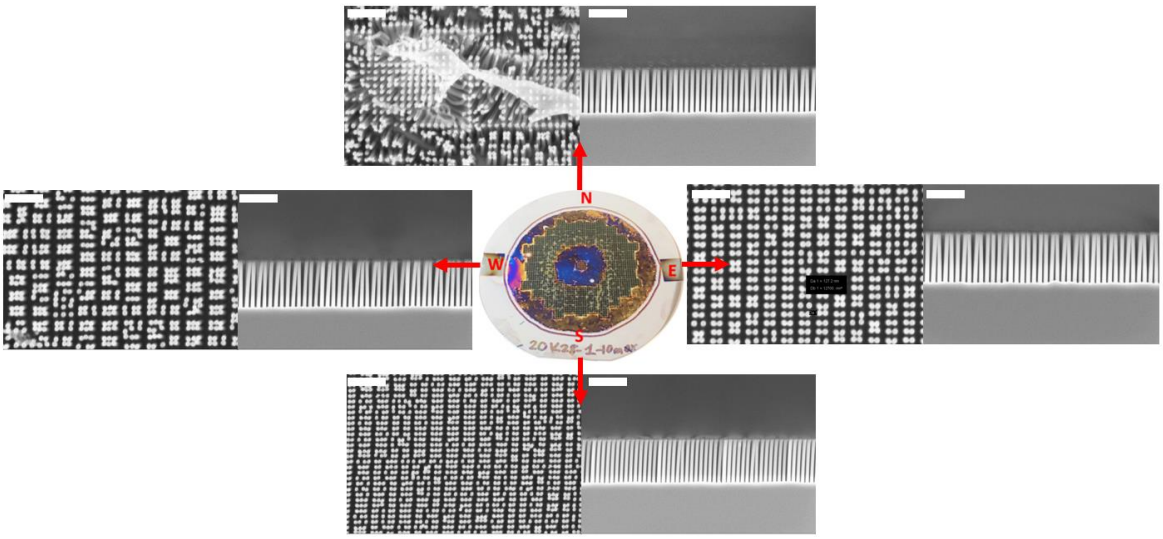


Figure 3.5: Oxide layer thickness – 10 nm showing top-down and cross-section views of N, S, E W (12.5M HF and 1M H_2O_2)

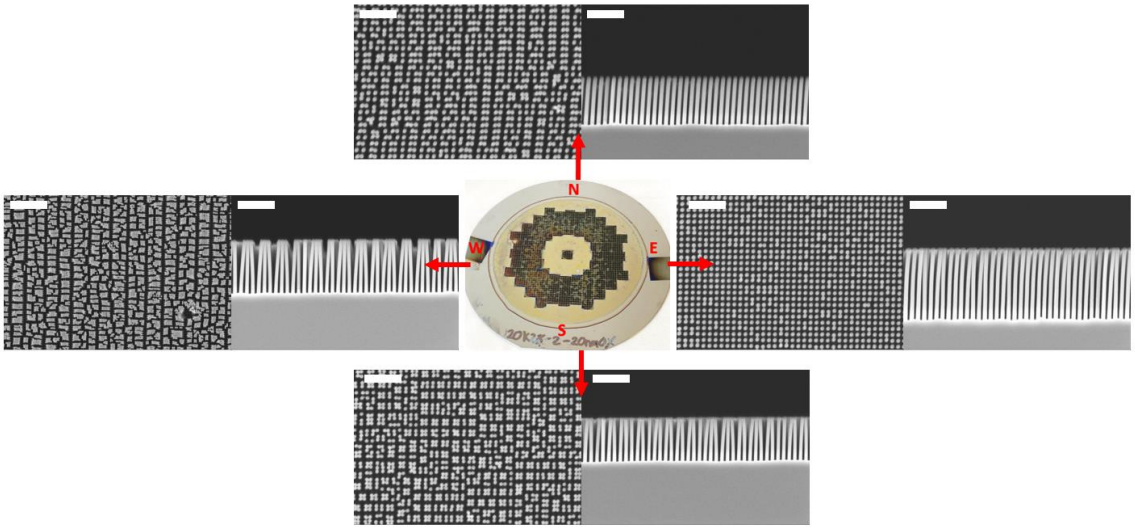


Figure 3.6: Oxide layer thickness – 20 nm showing top-down and cross-section views of N, S, E W (12.5M HF and 1M H_2O_2)

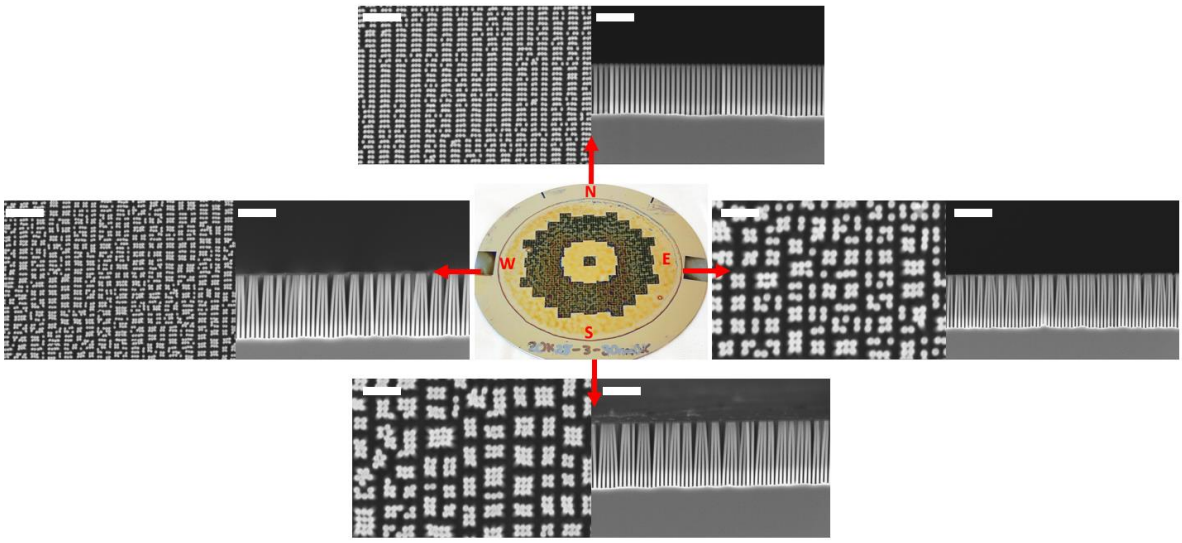


Figure 3.7: Oxide layer thickness – 30 nm showing top-down and cross-section views of N, S, E W (12.5M HF and 1M H_2O_2)

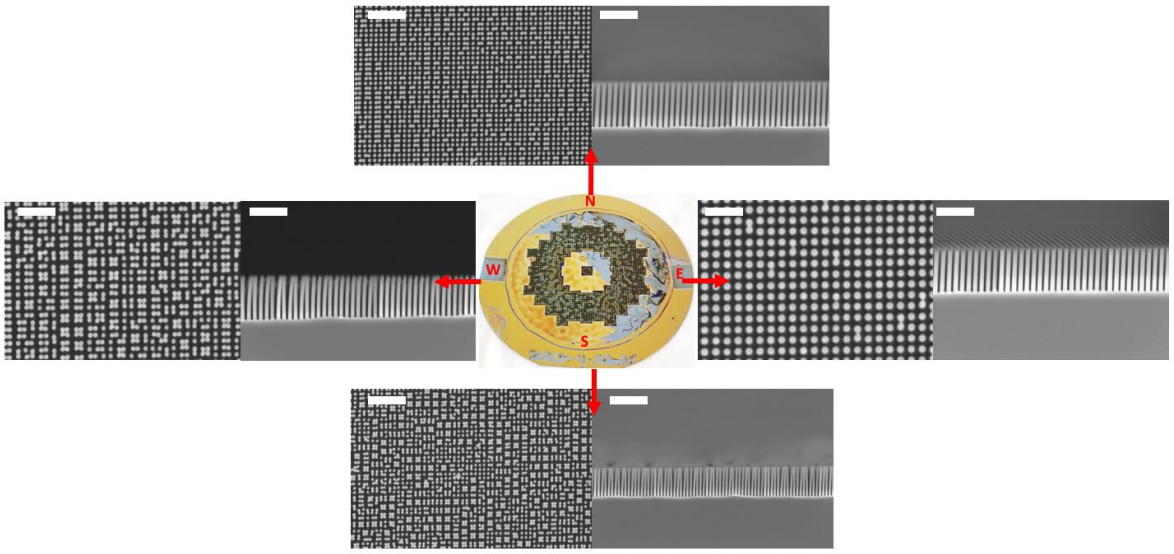


Figure 3.8: Oxide layer thickness – 50 nm showing top-down and cross-section views of N, S, E W (12.5M HF and 1M H_2O_2)

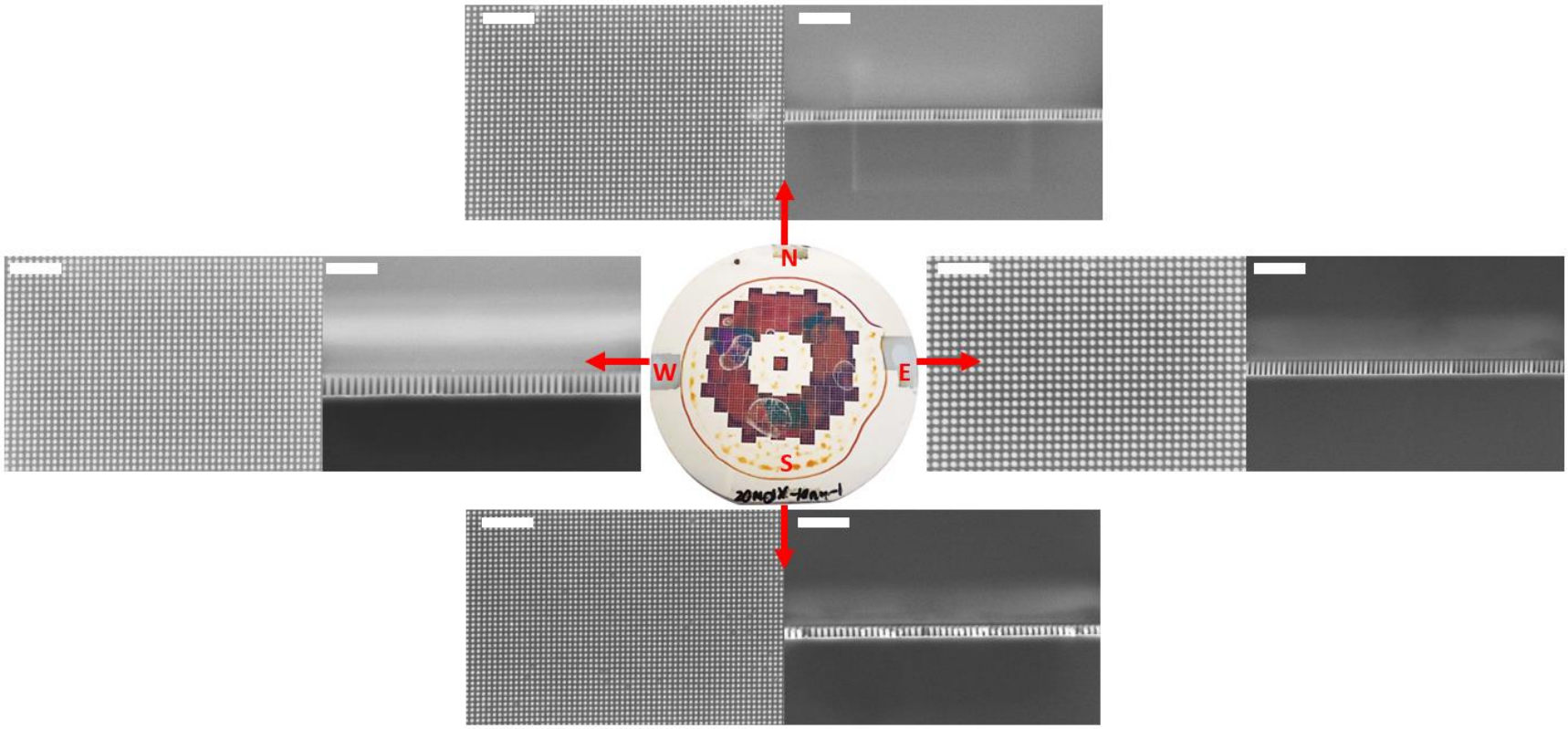


Figure 3.9: Oxide layer thickness – 10 nm showing top-down and cross-section views of N, S, E W (6.25M HF and 0.5M H_2O_2)

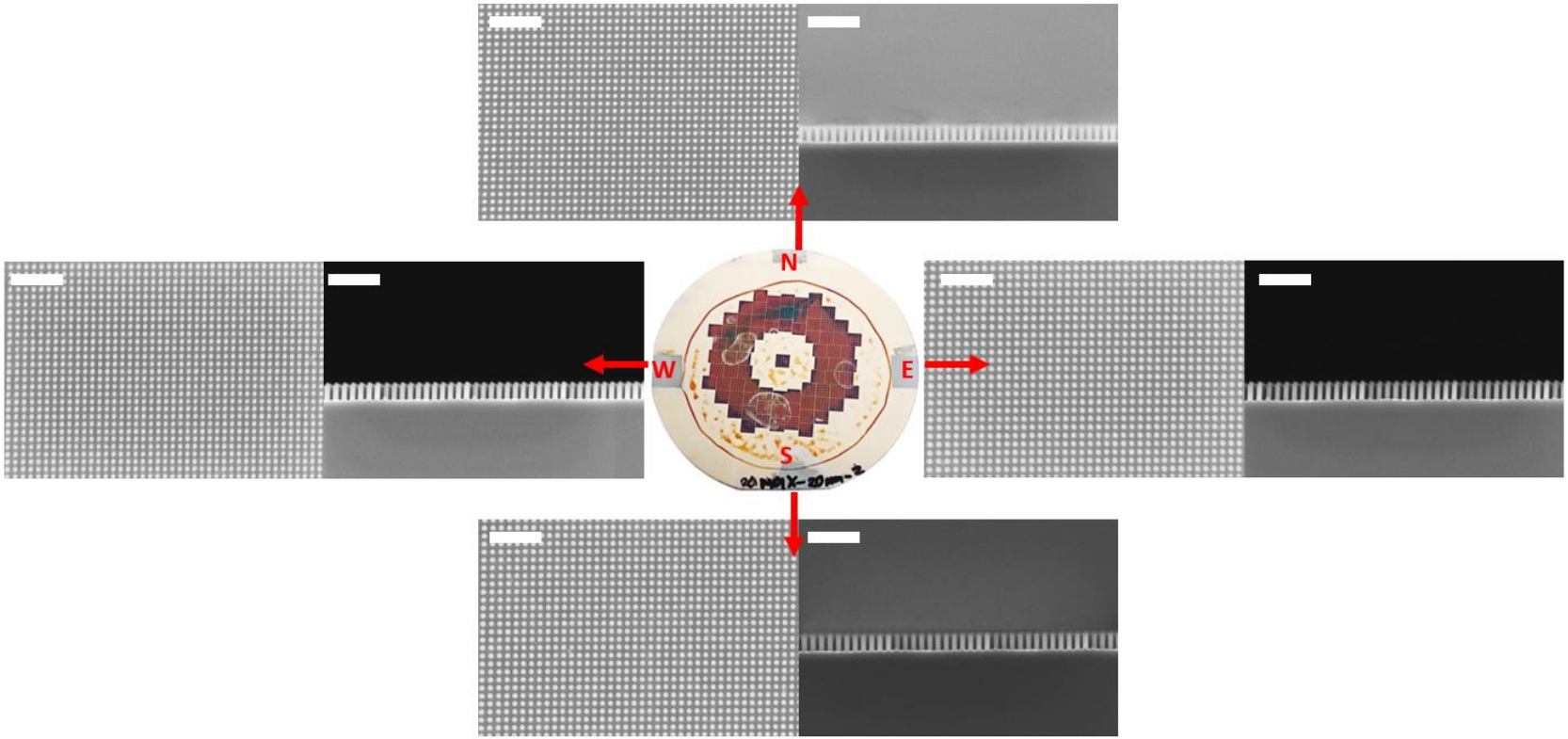


Figure 3.10: Oxide layer thickness – 20 nm showing top-down and cross-section views of N, S, E W (6.25M HF and 0.5M H_2O_2)

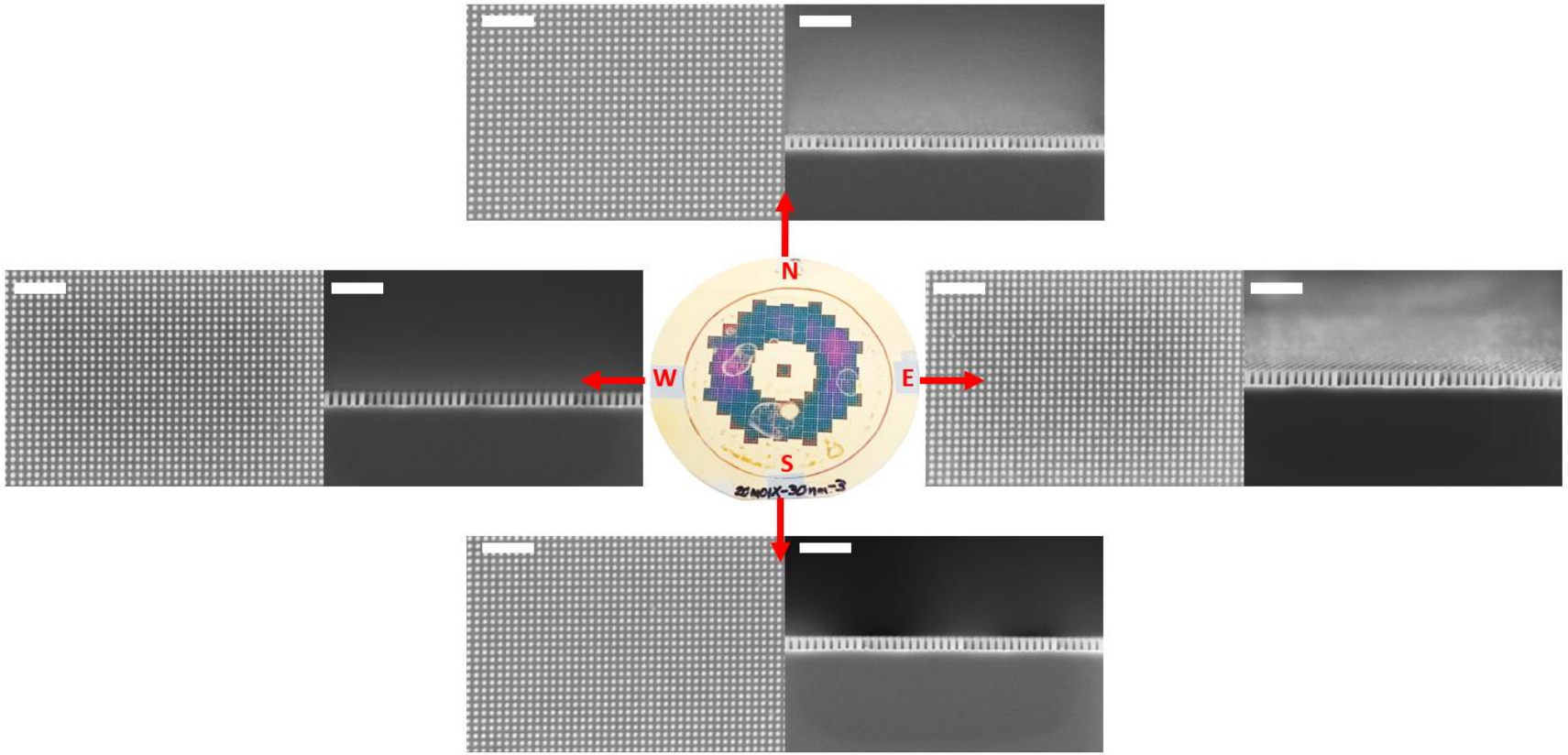


Figure 3.11: Oxide layer thickness – 30 nm showing top-down and cross-section views of N, S, E W (6.25M HF and 0.5M H_2O_2)

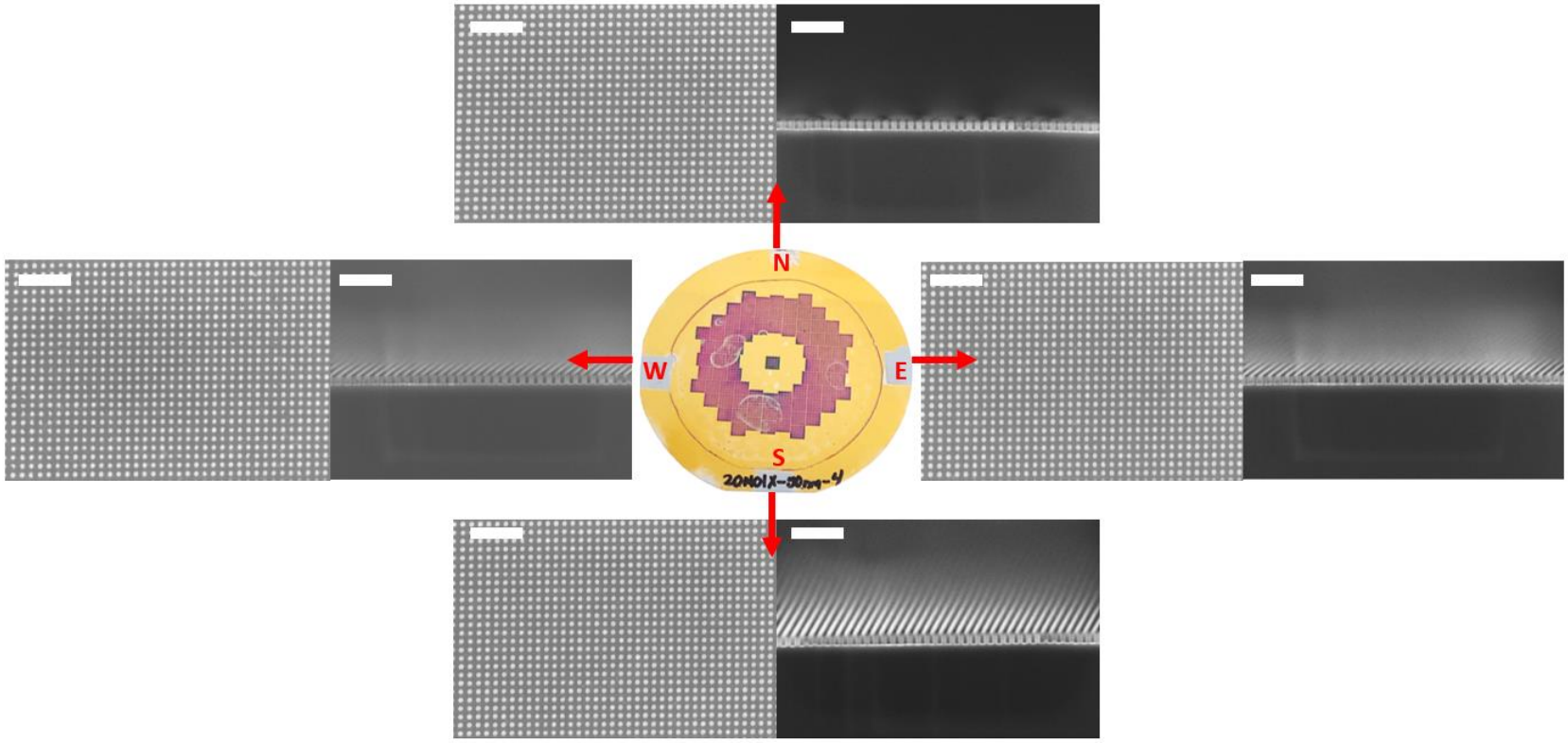


Figure 3.12: Oxide layer thickness – 50 nm showing top-down and cross-section views of N, S, E W (6.25M HF and 0.5M H_2O_2)

Table 3.2: SiNW dimension measurement and collapse comparison between Non-Diluted/Diluted MACE solution concentration

Oxide Layer Thickness	**MACE Solution Concentration**	**Avg. SiNW Height *h* (nm)**	**Standard Deviation σ_h (nm)**	**Avg. SiNW Diameter *d* (nm)**	**Standard Deviation σ_d (nm)**	**Collapse (Y/N)**
10 nm	*Non-Diluted MACE*	1695.77	79.84	121.18	3.52	**Y**
	Diluted MACE	487.40	89.49	116.56	9.81	**N**
20 nm	*Non-Diluted MACE*	1904.23	350.05	118.23	6.30	**Y**
	Diluted MACE	431.98	35.48	115.64	8.40	**N**
30 nm	*Non-Diluted MACE*	2697.77	454.53	117.18	11.98	**Y**
	Diluted MACE	355.18	17.98	115.55	6.77	**N**
50 nm	*Non-Diluted MACE*	1589.54	210.48	113.14	11.81	**Y**
	Diluted MACE	225.46	40.62	116.85	6.14	**N**

For both MACE concentrations, each Si wafer of different oxide layer thickness was submerged for a 30 second etch with the patterned side facing up. Then, the wafers were submerged in DI-H_2O to quench the etch and dried using a dry air supply. There were 25 data points for SiNW height measurements and 25 data points for SiNW diameter measurements per oxide thickness for the two MACE solution concentrations. The values used to calculate SiNW height, diameter, and standard deviation were averaged across all four locations (N, S, E, and W) of the wafer.

As observed with the Si coupons in the previous section, the (1) non-diluted MACE solution allowed for a high-speed etch rate, while the (2) diluted MACE solution produced a slower etch rate that yielded shorter SiNW heights. Table 3.2 shows the comparison in SiNW heights and feature diameters. For the diluted MACE solution, an interesting trend was perceived. As the oxide layer became thicker, the SiNW heights became increasingly shorter (10 nm oxide thickness = 487.40 nm SiNW height, 50 nm oxide thickness = 225.46 nm SiNW height). While collapsed nanowire arrays create "bundles" and a "black" Si color, non-collapsed nanowire arrays create diversification of colors like purple, green, and red, as Figures 3.9 – 3.12 show. These color variations are created because of the reflectance of different SiNW heights. Similarly, the "black" Si color in Figures 3.5 – 3.8 is a result of decreased reflectance across the visible spectrum [40].

During the diluted MACE of the 50 nm oxide thickness sample, there was a delayed start to the etch towards the last 10 seconds. During the first half of the etch, color variation was not present, suggesting that the 50 nm oxide layer was too thick to etch completely and allow for Si/catalyst etch in 30 seconds. Furthermore, the decrease in SiNW height

occurred because although the oxide layer is etched in HF, the solution took longer to etch through the oxide and the Si/catalyst interface. The oxide layer thickness was a successful and necessary step to induce uniformity across the wafer and prevent SiNW collapse because the oxide layer provided a consistent starting point for the etch, and allowed for uniform etchant transport to occur, despite the various oxide thicknesses. SiNW diameter fidelity was also characterized by local SEM images across the wafer. While SiNW heights were affected by different MACE solution concentrations, diameter shape fidelity was not primarily affected and was uniform across samples and MACE solution concentrations, with the two considerable variations being in the non-diluted MACE solution samples 10 nm and 50 nm oxide thicknesses as shown in Table 3.2.

Chapter 4: Summary of Research and Future Work

4.1 Conclusions

This thesis demonstrated the nanofabrication of Silicon nanowires enabled by nanoimprint lithography and MACE. An optimized metal break process was studied along with an oxide layer to create a consistent and uniform wafer-scale etch starting point that yielded high aspect ratio nanostructures. An initial process window of 0 nm – 100 nm oxide layer thickness was fabricated on a small-area Si coupon to investigate the etch depth uniformity, SiNW height, and NW collapse. The results from the initial experiments suggested a narrower process window. Subsequently, a process window of 10-50 nm was chosen for further investigation on full wafers. The MACE solution concentration was also varied to optimize the results. Results from the second set of experiments demonstrated scalability of the MACE process, depth uniformity, SiNW height, and NW collapse. The following section describes future work on the presented research in this thesis.

4.2 Future Work

Future research includes conducting a series of full-wafer MACE experiments with the diluted MACE solution for different etch times starting at 30 seconds with intervals of 30 seconds to achieve high aspect ratio SiNWs without collapse. In this thesis, local SEM was used to characterize and measure SiNW heights and diameters. However, SEM is a destructive method of metrology and affects the throughput of full-wafer MACE manufacturing and has an extremely limited field of view for larger samples. Scatterometry

and spectral imaging [41] could be implemented to avoid sample destruction and significantly increase throughput simultaneously.

An exemplar device application is now discussed. Ultra-high aspect ratio fabrication of deep capacitors for dynamic random-access memory (DRAM) requires deep and precise etching at sub-20 nm half-pitch structures. The shrinking of capacitor dimensions beyond 20 nm half-pitch requires a simultaneous increase in capacitance density to store the same digital data efficiently. There are three main factors that can be combined to address the demand for higher capacitance: increasing capacitor surface area, decreasing the dielectric thickness, and increasing the dielectric constant of the insulating layer [42]. Previous solutions of increasing capacitor area have utilized three-dimensional structures, like trenches or more complicated geometries. Therefore, to ensure enough capacitance, the aspect ratio of the trenches must be increased [43]. The feasible aspect ratios are reaching their limits due to two specific problems with reactive ion etching (RIE) processes at sub-20 nm feature sizes: (1) side wall angles in RIE etching are always <90 degrees leading to aspect ratio limits for sub-20nm holes; and (2) side-wall damage in deep holes lead to lack of crystallinity in pure silicon at the side walls.

Kim et al., detailed how MACE has allowed for the manufacturing of ultra-high aspect ratio semiconductor nanohole arrays with diameters ranging from 900 nm down to sub-100 nm [44]. Li et al. detailed the use of anodic MACE of silicon in which an electric field is applied to guide the etching of silicon using gold [6]. The process of fabricating high aspect ratios using MACE, which requires discrete dot catalyst patterns, is an important technique that can be applied to high density 3D memory, [45] interconnects

through silicon vias (TSVs), photonic crystals, detectors, and many other technologies. MACE has demonstrated near-vertical wall angles with no discernable damage as compared to RIE, and it has demonstrated sub-5nm shape control. However, creating holes in MACE leads to two main challenges: (i) catalyst wandering causing non-ideal holes that do not etch vertically down, which is not a problem in pillars as the catalyst is an interconnected mesh which does not wander; (ii) etch reactants have to be removed efficiently from deep sub-20nm holes which cause severe chemical transport problems at aspect ratios exceeding 100:1. These two MACE challenges need to be explored further.

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